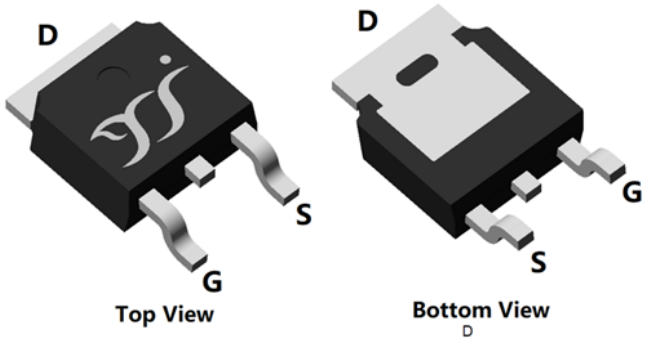
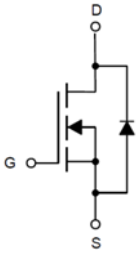
N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View

TO-252



Product Summary

- V_{DS} 200V
- I_D 11.4A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜280mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	200	V
Gate-source Voltage			V_{GS}	-30	30	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	1.9	A
		T_A=100℃,V_{GS}=10V		-	1.2	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	11.4	
		T_C=100℃,V_{GS}=10V		-	7.2	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	45.6	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		11.4	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=0.5mH,I_{AS}=18.9A		EAS	-	89.3	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.5	W
		T_A=100℃		-	1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	85.6	
		T_C=100℃		-	34.2	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.46	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD280N20AJ	F2	YJD280N20AJ	2500	/	25000	13“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	200	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=200V,V_{GS}=0V,Tj=150℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	1.3	2.1	2.9	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=4.5A,Tj=25℃	-	210	280	mΩ
Diode Forward Voltage	V_{SD}	I_S=9A,V_{GS}=0V,Tj=25℃	-	0.92	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	2.8	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V,f=1MHz,Tj=25℃	-	655	-	pF
Output Capacitance	C_{oss}		-	43	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=100V,I_D=4.5A,Tj=25℃	-	13.7	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	
Gate-Drain Charge	Q_{gd}		-	3.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=4.5A,di/dt=100A/μs,V_{GS}=0V, V_R=100V,Tj=25℃	-	300	-	nC
Reverse Recovery Time	t_{rr}		-	80	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=100V,I_D=4.5A,R_{GEN}=3Ω, Tj=25℃	-	5.8	-	ns
Turn-on Rise Time	t_r		-	2.9	-	
Turn-off Delay Time	$t_{D(off)}$		-	18	-	
Turn-off Fall Time	t_f		-	4	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

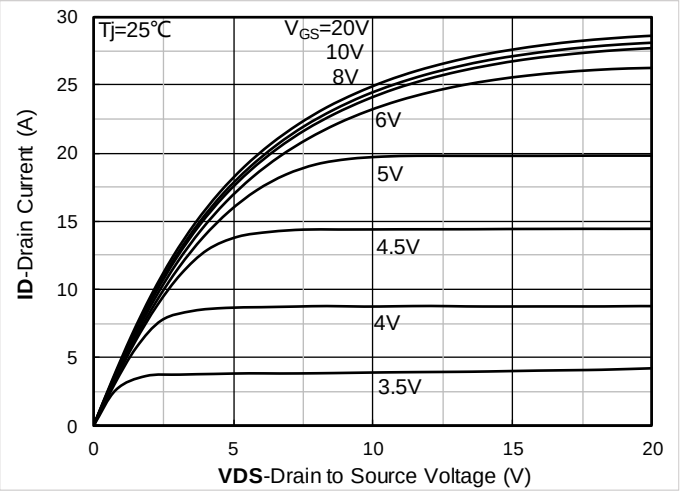


Figure 1. Output Characteristics; typical values

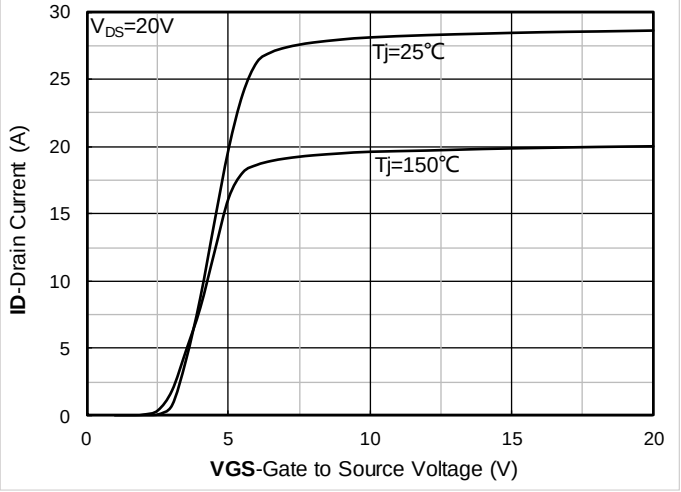


Figure 2. Transfer Characteristics; typical values

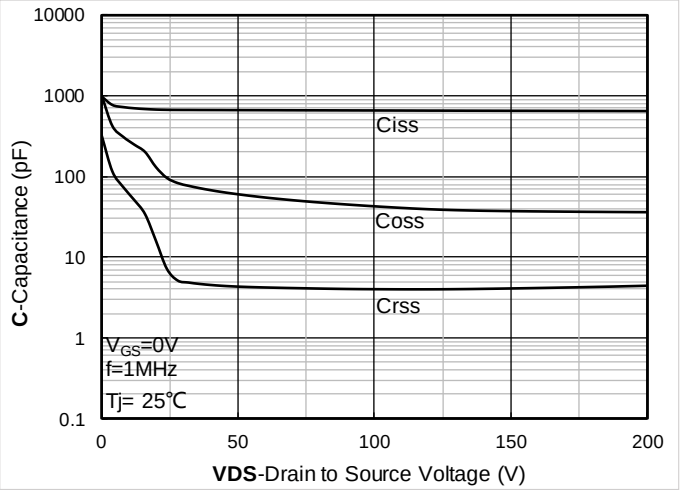


Figure 3. Capacitance Characteristics; typical values

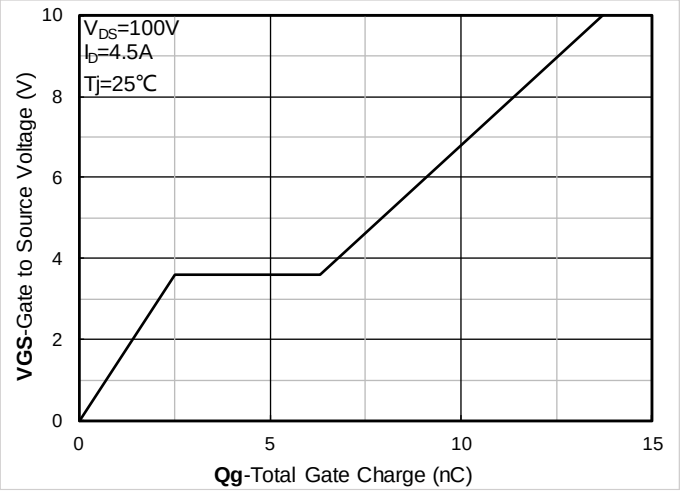


Figure 4. Gate Charge; typical values

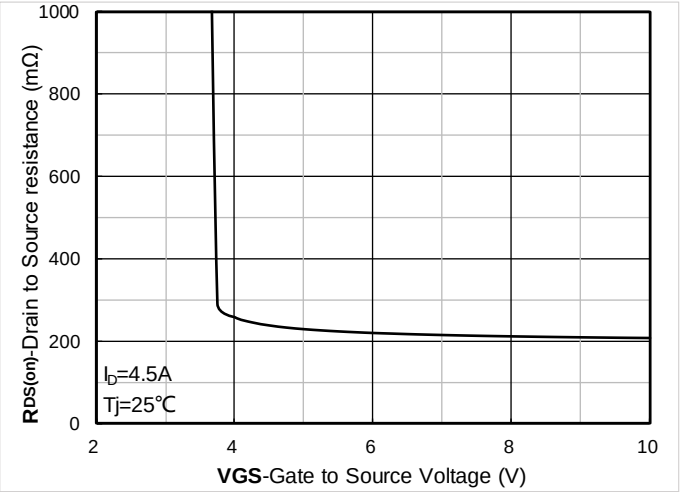


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

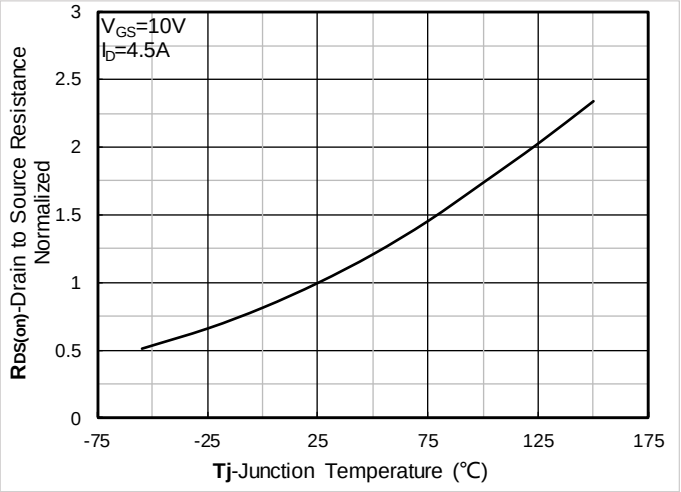


Figure 6. Normalized On-Resistance

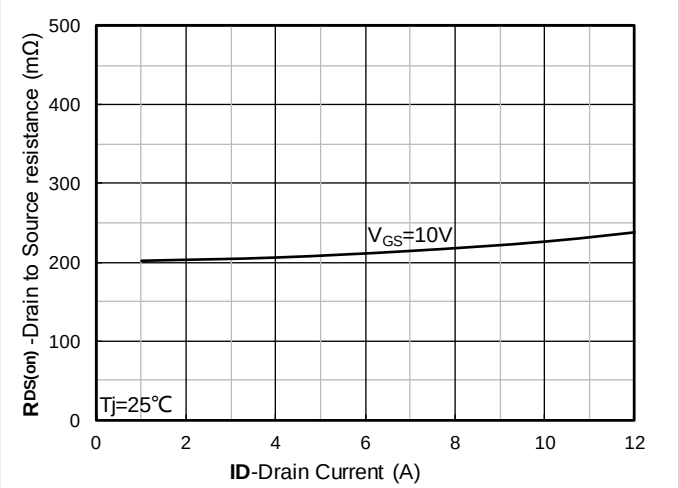


Figure 7. RDS(on) vs. Drain Current; typical values

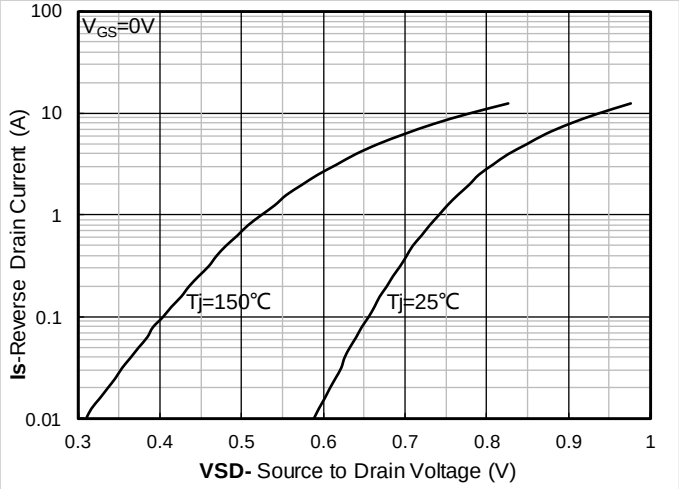


Figure 8. Forward characteristics of reverse diode; typical values

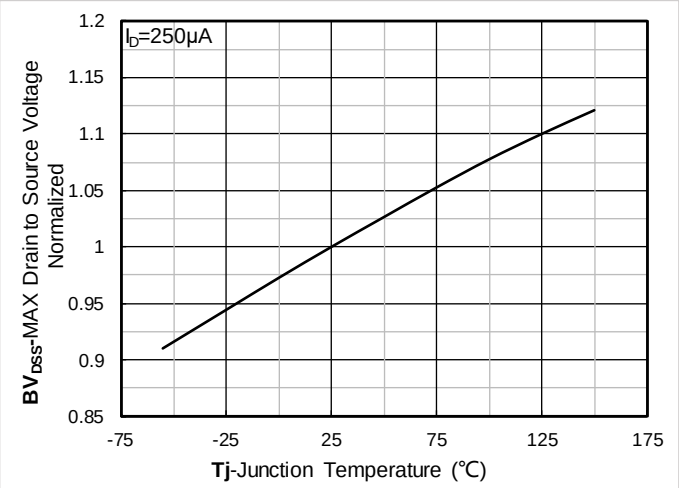


Figure 9. Normalized breakdown voltage

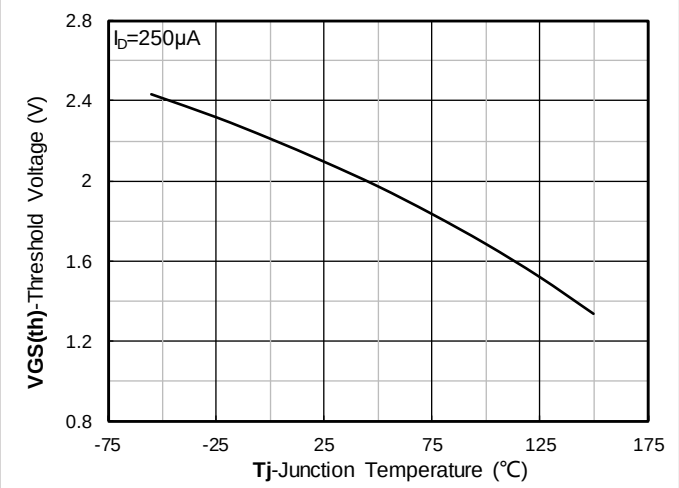


Figure 10. Gate Threshold voltage; typical values

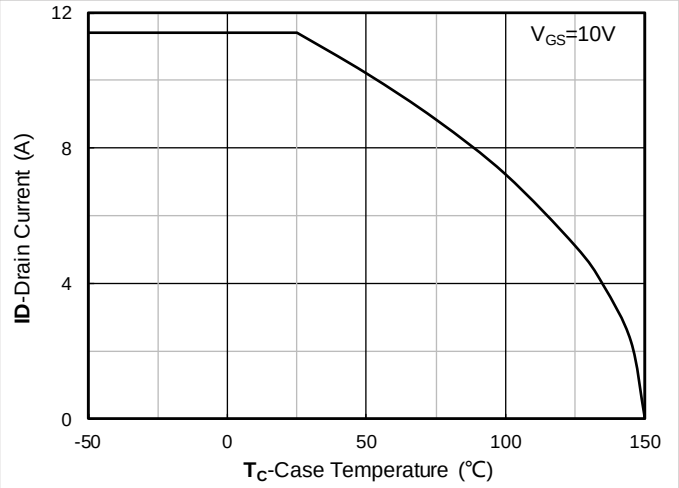


Figure 11. Current dissipation

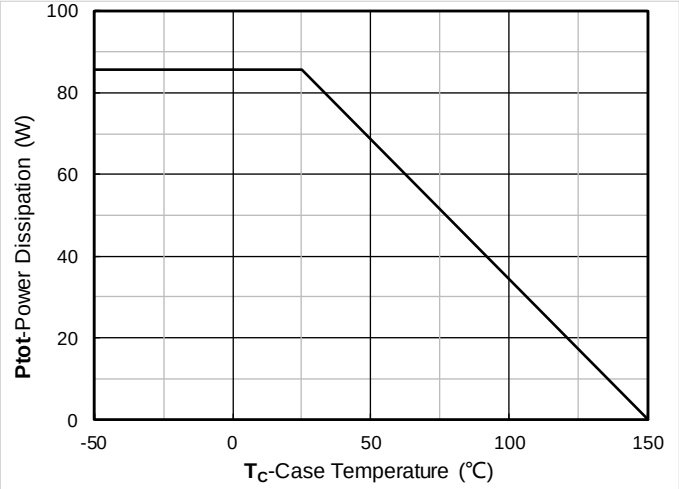


Figure 12. Power dissipation

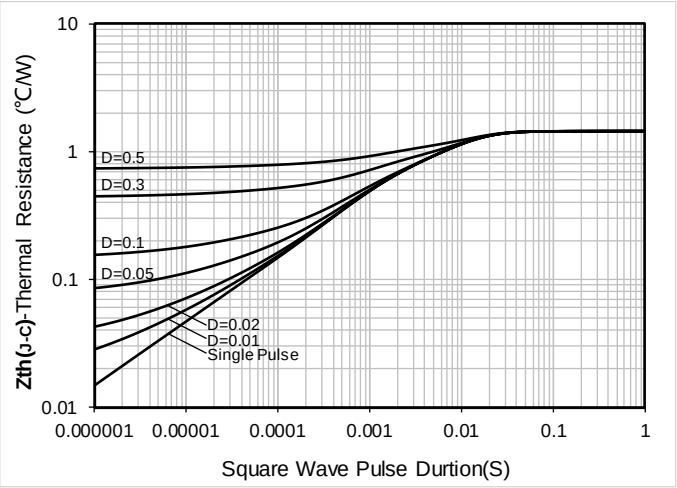


Figure 13. Maximum Transient Thermal Impedance

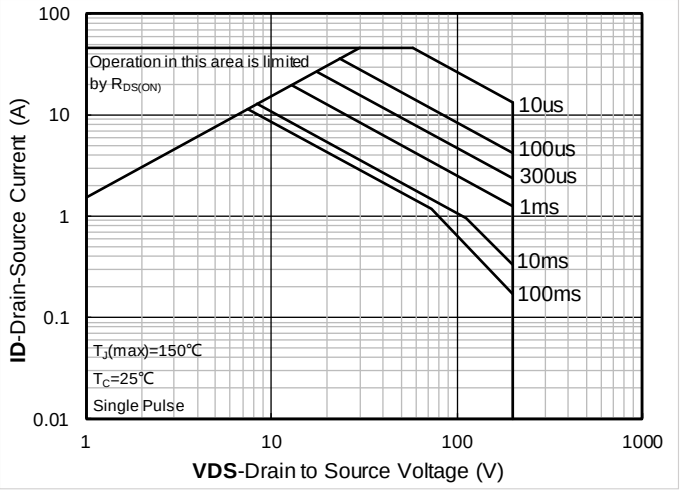


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

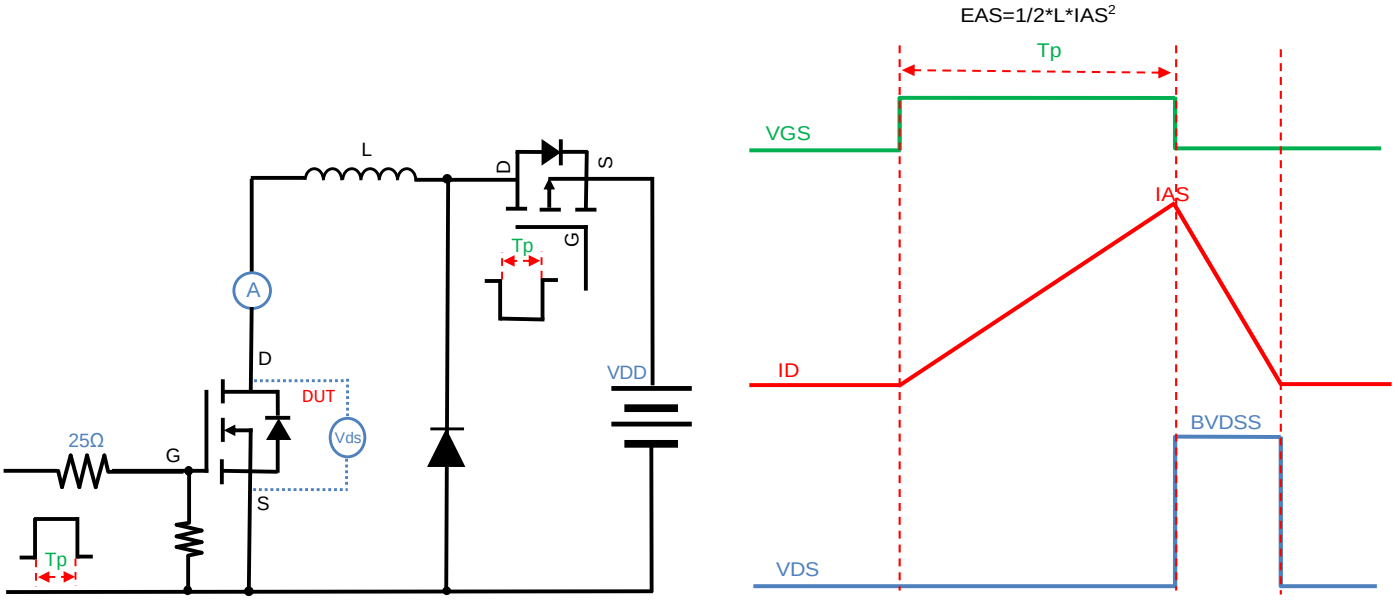


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

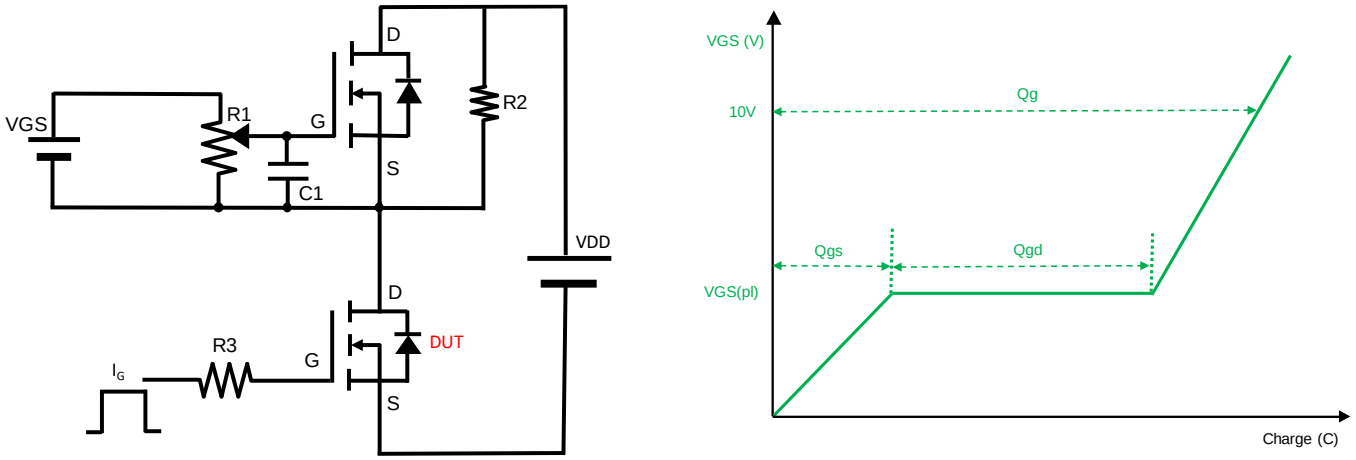


Figure B. Gate Charge Test Circuit & Waveform

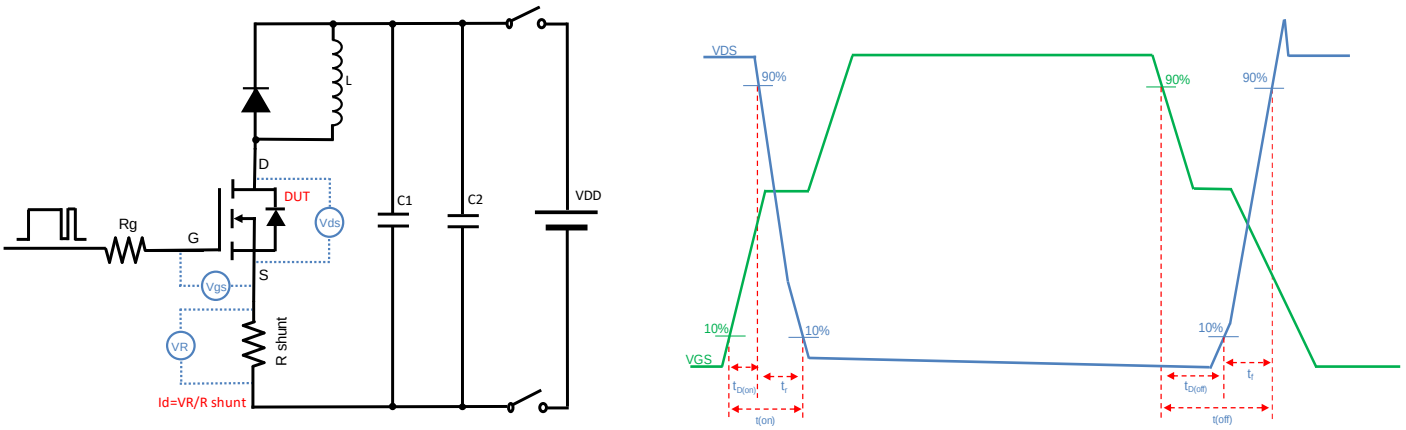


Figure C. Resistive Switching Test Circuit & Waveform

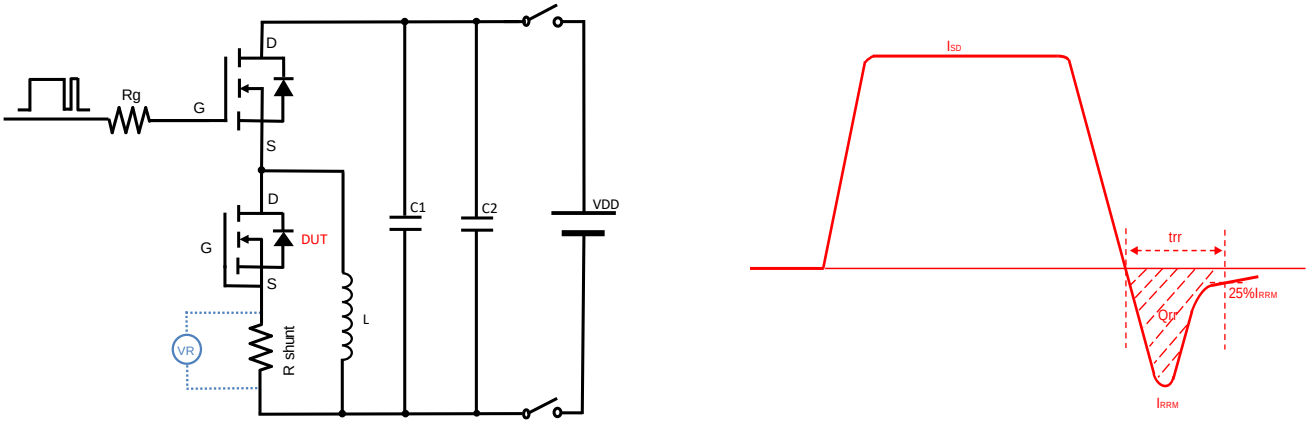
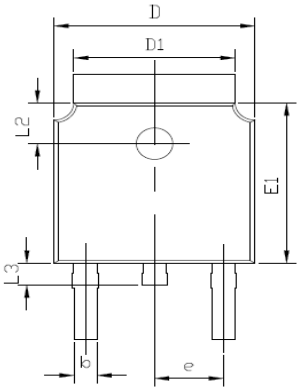
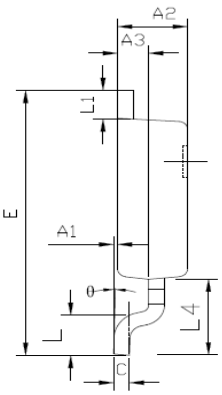


Figure D. Diode Recovery Test Circuit & Waveform

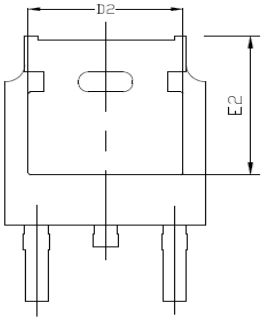
■ TO-252-B Package information



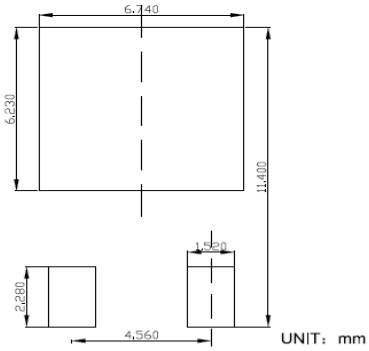
TOP VIEW



SIDE VIEW



BOTTOM VIEW

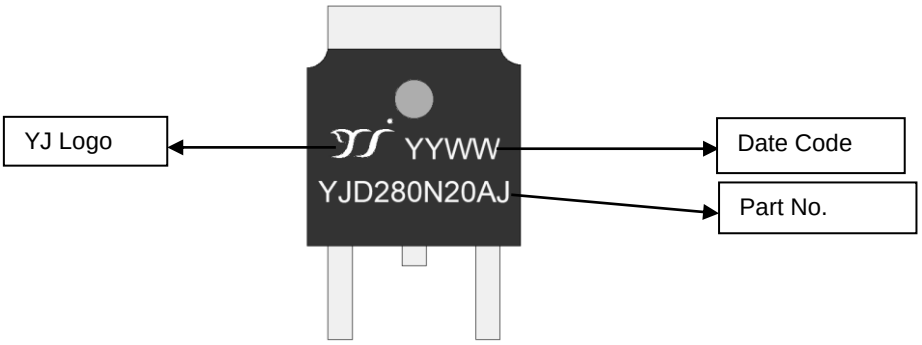


SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.000	0.008	0.000	0.200
A2	0.087	0.094	2.200	2.400
A3	0.035	0.043	0.900	1.100
b	0.026	0.034	0.660	0.860
c	0.018	0.023	0.460	0.580
D	0.256	0.264	6.500	6.700
D1	0.203	0.215	5.150	5.450
D2	0.181	0.195	4.600	4.950
E	0.390	0.406	9.900	10.300
E1	0.236	0.244	6.000	6.200
E2	0.203	0.215	5.150	5.450
e	0.090BSC		2.286BSC	
L	0.049	0.069	1.250	1.750
L1	0.035	0.050	0.900	1.270
L2	0.055	0.075	1.400	1.900
L3	0.024	0.039	0.600	1.000
L4	0.114REF		2.900REF	
θ	0°	10°	0°	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■ Marking Information



Note：
1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJD280N20AJ is part no., YYWW is date code, “YY” is year, “WW” is week
4. Body color: Black

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The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

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